CIRCUIT AS A SENSOR, A PRACTICAL CONCEPT FOR ELECTRONIC PROGNOSTICS

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Abstract: Practical condition assessment and prediction of remaining useful life for electronic communication and weapon systems offers significant potential for improved readiness and field reliability of military and civilian defense systems. Modern systems, operating in the Radio Frequency (RF) spectrum, employ significant digital signal processing and data management elements central to their core design purpose, offering an opportunity to exploit available data for condition monitoring and health assessment. These Digital RF (RF/D) systems have become ubiquitous in Department of Defense (DoD) and in civilian life including systems such as radar, GPS and communications. As the importance of these systems has increased and designers seek to embed apertures and dynamic circuit elements into weapon platform structures, maintainability and reliability become significant concerns. The authors have developed and demonstrated techniques for RF/D Prognostics and Health Management (PHM) that can help reduce significant costs resulting from traditional maintenance techniques. This paper introduces the 'circuit as sensor' concept as an innovative PHM solution that minimizes or eliminates the need for additional sensor and data acquisition equipment to implement PHM on RF/D systems. System level features and device functionality data provide failure prediction and RUL estimation. Results from ongoing research and development are presented.

Keywords: Diagnostic features; electronic systems PHM; failure prognostics; radio frequency / digital circuits; remaining useful life

Introduction: Existing diagnostic and condition assessment technology for defense applications include built-in self-test, at-wing performance and diagnostic test, and depot-level test and recertification. While these are functional from a historic perspective, they currently yield no prognostic capability. The adequacy of the current technology to quickly detect problems, isolate root cause and maximize availability is severely stretched while supporting a high wartime op-tempo and an aging fleet. Moreover, PHM has now become a requirement for defense systems.

This "circuit as sensor" approach enables a PHM solution that minimizes or eliminates the need for additional sensor and data acquisition equipment. An embedded prognostic capability that builds on existing operational data and leverages emerging physics of failure modeling with anomaly detection and component degradation characterization provides a significant opportunity to enhance and improve the operational availability and logistical support infrastructure for deployed and emerging weapon systems.

Proposed Approach: Impact Technologies, LLC (Impact) has to developed and demonstrate the ‘circuit as a sensor’ concept as an innovative PHM solution for mixed mode radio frequency / digital (RF/D) electronic systems. The RF/D domain refers to those systems that use radio waves (15 kHz to 300 GHz portion of the electromagnetic spectrum) with digital signal processing. Utilizing sound engineering principles and building on diligent study of physical failure mechanisms, the developed electronic PHM technology leverages existing circuit operational data as a basis for prognostic feature extraction and provides a high confidence component health index. This index reflects the component current operating condition and establishes the foundation for RUL prediction. Figure 1 outlines the RF/D PHM concept.

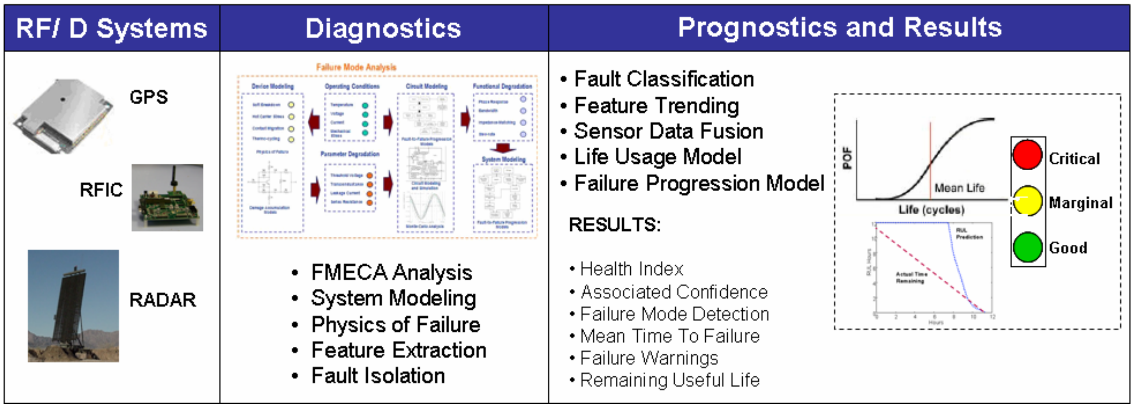

Figure 1: Conceptual Diagram for RF/D PHM

First diagnostics is performed using the conventional Failure Mode Effects and Criticality Analysis (FMECA) which identifies causes of system failure by performing device-level, circuit-level, and system-level modeling. FMECA and mathematical physics of failure models help analyze parameter degradation resulting from damage accumulation for each device. These derived prognostic features update life usage and failure progression models upon which classifiers and inference engines deliver the overall health prognosis. Intelligent fusion of prognostic features serves to increase robustness and decrease prediction uncertainty. The ability to monitor and predict failures, detect and classify anomalous events, and assess remaining useful life in RF/ D systems can provide significant cost benefits, enhanced mission readiness and condition based maintenance.

The ensuing sections outline a simulation study aimed at analyzing the effects of critical component degradation on RF communication systems. In addition, a hardware experimental investigation is also presented for the validation of Cyclic Redundancy Check (CRC) as a system level metric for fault detection.

Simulation of a QAM communication system: Previous investigatory studies have revealed that in a mixed mode communication system, the RF front end analog circuitry is more susceptible to damage than the digital circuits of the system [2]. The authors started out by creating a Simulink model of a Quadrature Amplitude Modulation (QAM) communication system. The primary objective of the simulation was to catalog the effects of component degradation on communication system functionality. The secondary objective was to ascertain access points and potential features that can be used for the detection of degraded performance. QAM was selected because it is extensively used in wireless communications (for example systems using the IEEE 802.11 standard).

In QAM, the amplitude of two sinusoidal waves, 90 degrees out-of-phase with each other (in quadrature) are modulated or keyed to represent the data signal. The signal constellation (or I/Q plot) for 16 – QAM consists of 16 points. Therefore this modulation scheme allows a user to transmit four bits per symbol (4 bps) [3]. A Simulink® block diagram of the QAM system developed for the study is shown Figure 2. A digital data generator is used to create a pseudo random bit stream for transmission. This bit stream is fed to a rectangular QAM block which produces the corresponding in phase/quadrature signals. At this point a custom up conversion block modulates the I/Q signals onto the carrier wave. A similar down conversion and demodulation process is used to extract the digital message. RF impairment blocks and noise blocks were added to the simulation to estimate the effects of damage accumulation in sensitive front end RF components. An error rate calculation block was added to provide an estimate of Signal to Noise Ratio.

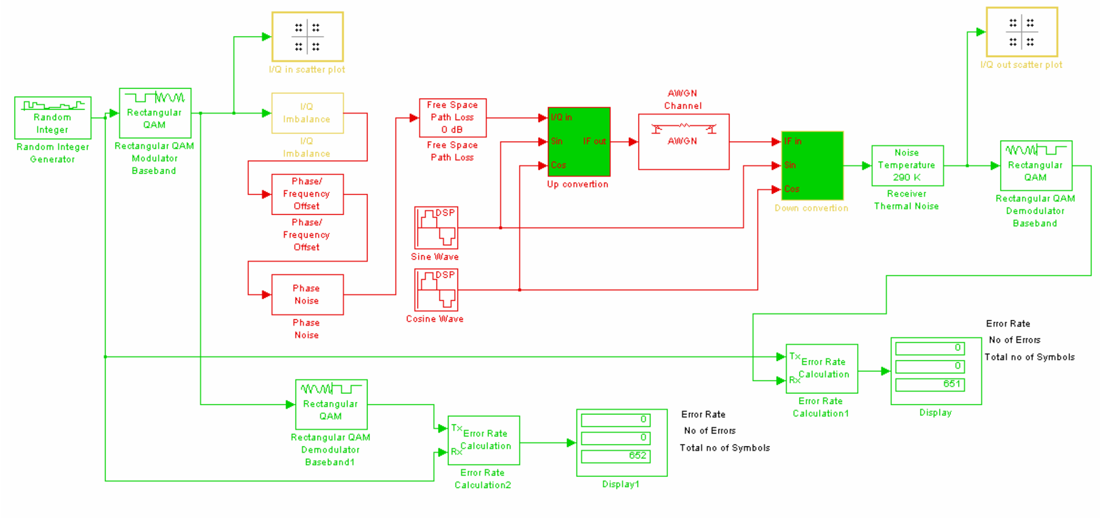

Figure 2: 16 - QAM System (Simulink Model)

Simulation results: A snap shot of the I/Q plots from one of the simulation runs is presented in Figure 3. The left half side of the figure shows a healthy I/Q constellation with the correct point spacing. The right half shows a cluster of received data points. Amplitude and phase misalignment effects can clearly be observed in the right hand side plot. The effects of the Additive White Gaussian Noise (AWGN) block can also be observed. Transmitted RF signals undergo similar distortion effects due to degradation of critical RF components.

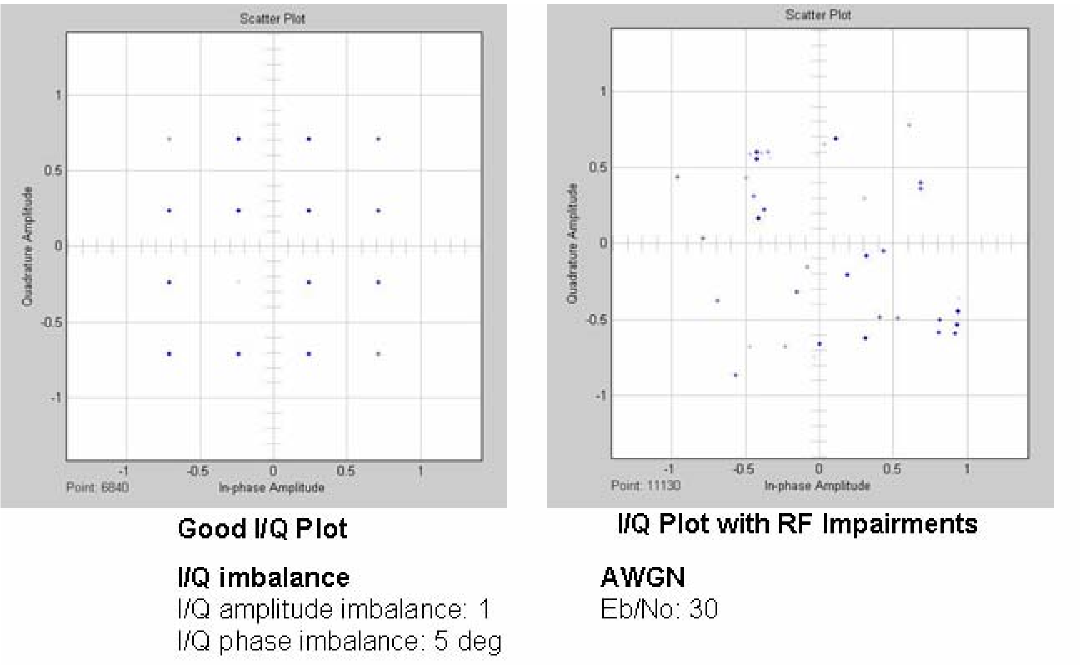

Figure 3: I/Q plots with and without RF Impairments

In practice, the receiver unit calculates the Euclidian distance between a newly received symbol and all the points in a predefined signal constellation (refer to equation (1)). A threshold setting is used to evaluate what symbol has been received [3].

$$D(y, S_m) = \| y - S_m \|^2, \ where\ m = 1,2,....16 \qquad (1)$$

This level of decision making is usually abstracted from the user of the communication system. Once the signal waveform has been demodulated, processing can be performed on the recovered digital data. The received bit stream is grouped into chunks called packets. Most modern day communication systems use a wide variety of packet handing schemes such as error checking, data whitening and Forward Error Correction (FEC) encoding/decoding. Error mitigation is done using Error Correcting Codes (ECC) or by performing Cyclic Redundancy Checks. These checking schemes are an in built or integral part of the communication system. Characterizing or trending CRC profiles of the received digital data as function of component degradation can provide Built- In- Test (BIT) capability. Fault isolation and prognostic information may also be extracted.

Cyclic Redundancy Check (CRC) as a feature: CRC is a checking procedure that identifies if broadcasted digital data has been corrupted during transmission. At the transmitter end, a CRC number is appended to the message data along with some additional bits to create a data packet (refer to Figure 4). At the receiver end, polynomial division is performed on the received packet to verify the integrity of the received data.

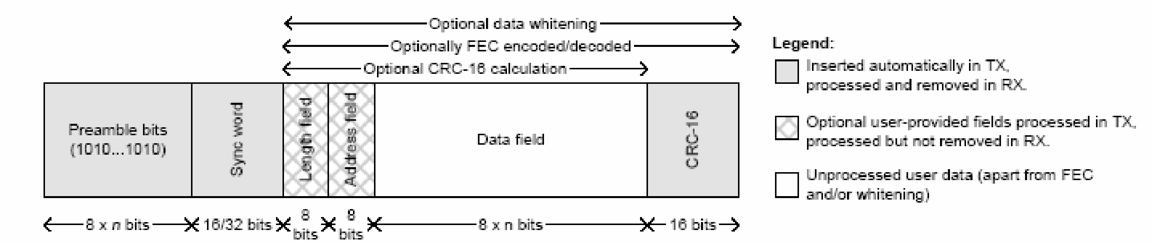

Figure 4: CRC Packet handling in the Chipcon CC2500 RFIC

The mathematical equation for CRC is easy to understand can be implement in software or in hardware using logic gates (refer to equation(2)).

$$M(x)\cdot x^{n} = Q(x)\cdot G(x) + R(x) \tag{2}$$

Where M(x) is the message polynomial,
Q(x) is the quotient,
G(x) is the CRC polynomial key,
R(x) is the remainder
n is the degree of the generator polynomial

The generator polynomial G(x) is predefined and known to both the transmitter and receiver units. The transmitting unit creates a data packet by appending the remainder R to the message bits M. The receiver unit computes the expression $M(x)\cdot x^{n} - R(x)$ and performs polynomial division with G(x) to check if the remainder of the operation is zero[8].

Such error checking schemes have long been used in the wireless industry to evaluate the performance of communication systems to meet design specifications. The use of such features for damage quantification, fault isolation and Remaining Useful Life estimation is a new and important research avenue. CRC has been identified as a feature that is useful as a precursor to failure in Radio Frequency IC’s. The subsequent sections discuss the experimental study that was conducted to validate CRC as a feature for self health assessment.

Test platform for experimental study: The CC2500 RFIC chip and SmartRF® 04 Evaluation Board System were selected for the hardware testing and experimentation. The evaluation system consists of two separate boards; a main board and a daughter board (refer to Figure 5 and Figure 6). The CC2500 RFIC provides a robust feature set allowing the user to select from various digital modulation schemes, data rates and packet handling schemes. Operating at a carrier frequency of 2.4 GHz the CC2500 also comes with frequency hopping capability. The system on chip QLP package houses both the analog RF and digital circuitry. Therefore the most logical method for diagnostic/prognostic analysis is by use of the black box methodology.

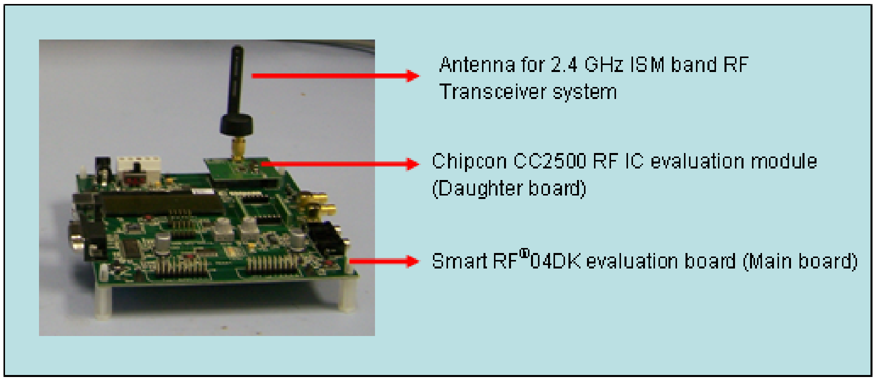

Figure 5: CC2500DK Evaluation Board

Figure 6: CC2500DK Evaluation Module or Daughter Board

The main board of the test system uses a Silicon Labs C8051F320 MCU to manage resources and to interface with the CC2500 RFIC chip. During testing an external PC or data acquisition computer can be connected to the main board via a USB port. Chicpon also provides SmartRF® Studio Software to interface with the CC2500 RFIC. This software was used to create the test profiles for the experiments and was also responsible for providing the output after the execution of the specified tests. Some of the test profile parameters (that were varied) were packet length, number of packets, modulation scheme and receive filter channel bandwidth.

For preliminary testing, temperature was selected as the stress factor for ageing the CC2500 RFICs. One of the objectives of the experiment was to figure out a ball park estimate of the stress conditions necessary to induce degraded communication performance.

Component ageing: A population of ten (10) RFIC chips was used for the failure testing. Five of these chips were seeded with faults by means of accelerated ageing. An APE rework station (refer to Figure 7) was used to age the CC2500 ICs. It provided an accurate method to control the temperature conditions that the chips were being subjected to. When compared to a conventional environment chamber, the APE rework station also has a significantly advanced thermal shocking capability. The five chips mentioned above were quantified to different levels of damage based on the time that they were subjected to elevated temperature conditions. Table 1 outlines the chips used in the study. Level 5 represents the maximum amount of damage and level 1 represents the least amount of damage.

Figure 7: APE Rework Station

Table 1: Damage levels of the CC2500 Chips

Damage level	Chip No.
Level 5	S10
Level 4	S9
Level 3	S8
Level 2	S7
Level 1	S6
Healthy	B5
Healthy	B4
Healthy	B3
Healthy	B2
Healthy	B1

Seeded Fault Testing: Seeded fault tests were conducted using a pair of boards as shown in Figure 8. The total distance for the test runs was 220 feet (in 20 feet increments). At each distance 4 preset configurations were tested. Presented in Table 2 are the settings for these configurations. One unit was connected to a PC for test initiation and data acquisition. This was called the master unit. The other unit was called the slave unit and was configured to function in the stand alone mode. The tests were defined so that each of the boards would transmit and receive predefined data streams. This was done to access the state of the transmit/receive components of both transceiver units.

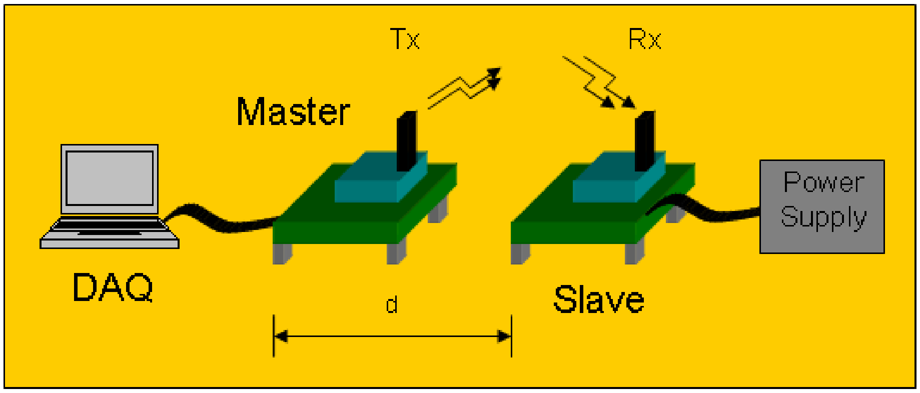

Figure 8: Range Testing

Table 2: List of Preset Configurations

Preset configuration	Data rate (kbps)	Modulation	RX filter bandwidth (kHz)
1	2.4	2-FSK	203
2	10	2-FSK	232
3	250	MSK	540
4	500	MSK	812

The tests were conducted indoors with bounded temperature and humidity conditions. For each transmission run, the test software recorded packet error information. The packet error information consists of two parts. The first being number of lost packets and the second being number of packets received with CRC errors. CRC information was being computed and reported by the CC2500 chip itself. This measurement was considered reliable because previous studies have indicated that analog RF components are nearly a hundred and fifty (150) times more susceptible to damage than digital circuitry subjected to same stress factors [2].

Experimental results: Overall functionality was accessed, by collectively analyzing the data gathered from the different test runs and preset configurations. Shown in Figure 9 and Figure 10 are the plots for total error vs. distance (for different levels of degradation). Baseline curves are marked with the letter ‘B’ in the legend and the seeded fault test curves are marked with the letter ‘S”. Chips 9 and 10 suffered complete communication failure but still retained digital functionality. It was possible to configure and write to the registers of chips 9 and 10. With the exception of chip 7, a clear distinction can be observed between baseline data and seeded fault test data.

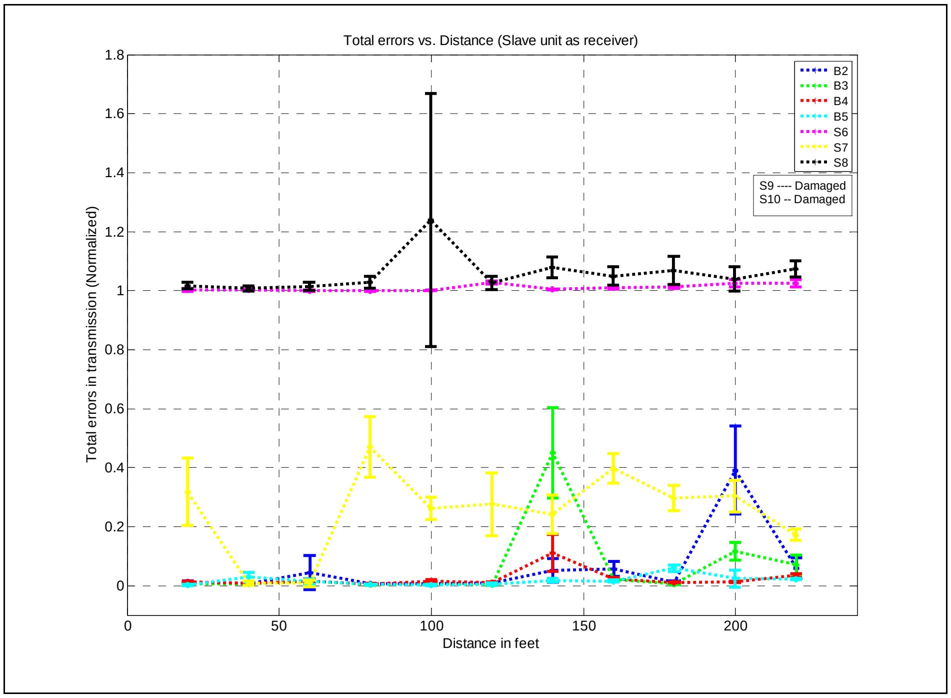

Figure 9: Slave as Receiver

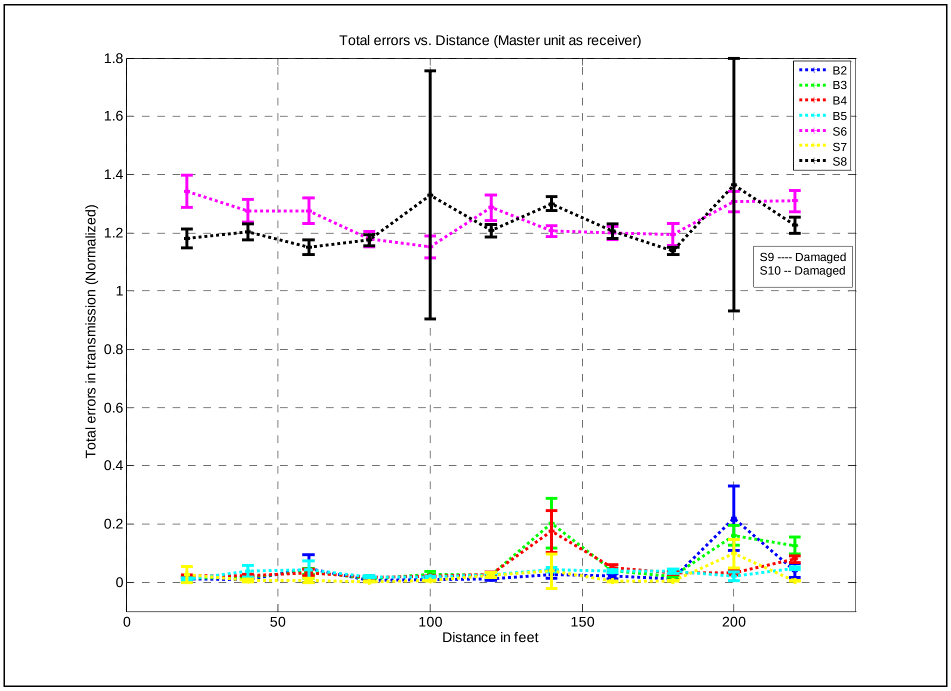

Figure 10: Master as Receiver

The preliminary goal of the experiment was to estimate the required damage level for noticeable performance loss. The presented experimental results confirm that CRC error profiles can be used as a metric to evaluate the health state of a digital RF communication system. Further more the minimal data spread, would allow for the implementation of a

BIT type detection system to provide users with a warning about the health state of the communication system. Most modern communication systems are designed with significant digital processing capability. Built in embedded test profiles can be used to trend features such as CRC during the life time of the communication system. This self damage detection and health assessment capability is the core foundation of the circuit as sensor concept. Additional experiments shall be performed to characterize the fault to failure progression and to provide RUL estimation capability.

Conclusion: The proposed circuit as sensor approach uses readily available system level features such as CRC profiles to detect degraded performance of communication systems. Preliminary trends have been established using the experimental data for damage level detection which is an important step towards implementing a Prognostic Health Management architecture for RF communication systems. This technology can be applied to broad class of electronic systems ranging from digital telephony, wireless networking, cellular communications and emergency radio systems to telemetry, guidance and control. The anticipated benefits include significant cost reduction through better lifecycle management, risk mitigation through increased system reliability, and better logistics support through condition based maintenance.

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